NOVATEK
聯 詠 科 技

Data Sheet

NT96223

Digital Still Camera Processor

Version 0.5

Table of Contents

Revision History

Rev.	Date	Author	Contents
0.3	2011/03/25	Kevin Hung	First draft version.
0.4	2011/06/21	Kevin Hung	Add electrical characteristic
0.5	2011/07/05	Kevin Hung	Add NT96223

Features

- High performance 32-bit CPU
  - □ ARM9DMI compatible
  - □ MPU built in
  - □ 4KB instruction and 4KB data cache
  - □ Embedded ICE makes firmware debugging easier
- Power-management features
  - □ Firmware configurable operating frequency of each functional block to meet best power budget
  - □ CPU operating frequency up to 240MHz, on the fly programmable
- Integrated clock generator
  - □ Internal phase-locked-loop
  - □ 12MHz system/USB crystal
  - □ 32768Hz RTC crystal
- Scaleable memory bus architecture
  - □ 16 bits SDRAM bus, supporting up to 256Mb SDR SDRAM die or 256Mb DDRI SDRAM die
- Sensor Interface Engine
  - □ Support up to 32M pixel sensor and the internal CMOS image sensor controller is programmable by the serial interface.
  - □ Support 10-bit CMOS sensor input
  - □ Support CMOS Image Sensor: OVT, Aptina, Samsung…, etc.
  - □ Sensor black level clamping
  - □ Efficient defect concealment algorithm
  - □ Raw image sub-sample for video
  - □ Gamma LUT
  - □ Flexible image analysis flow for AE, AF and AWB purpose
  - □ Flash light control
  - □ Lens shading and color shading compensation technology (patent pending)
  - □ Pixel binning for high ISO
  - □ In-pipe dark frame subtraction to reduce fixed pattern noise for capture mode
  - □ Defect columns and lines compensation
  - □ Support CCIR601 input
- Image Processing Engine
  - □ Proprietary anti-alias RGB Bayer CFA color interpolation

- □ Flexible edge rendering, control and enhancement
- □ Powerful noise reduction technology (patent pending)
- □ High precision color correction matrix for sRGB or specific color requirement
- □ Brightness/contrast and hue/saturation adjustment
- □ Specific color control technology (patent pending)
- □ RGB to YCbCr color space transform
- □ Same preview and capture paths
- □ False color suppression
- □ In-pipe special effects available

■ Image Manipulation Engine

- □ High quality scaling engine for digital zooming
- □ Forward/inverse color space transform
- □ Chroma filter for color noise suppression

■ Graphic Engine

- □ Copy and paste
- □ Geometric operation including mirror, flip, rotation and scale down
- □ Arithmetic operation including addition, subtraction, color keying, logic operation and alpha blending

■ JPEG Codec

- □ Support Motion JPEG 720P30(SDR) and 1080P24(DDR) video clip/playback function (Don't consider Card Speed)
- □ Support AVI file format
- □ Support ISO/IEC 10918-1 baseline JPEG compression/decompression. The still image resolutions up to 32M pixels
- □ Support downloadable Quantization and Huffman tables
- □ Support thumbnail image generation
- □ Support Exchangeable Image File format (EXIF 2.2)

■ LCD/TV display

- □ High performance scaling up/down engine and programmable gamma correction for display
- □ Support digital TFT LCD panel interface for AUO, Casio and Toppoly panels
- □ Support digital CSTN LCD panel interface
- □ Integrated TV encoder with DAC, support both NTSC/PAL composite video output
- □ Support dual panel display

■ 8-Bit digital video I/O port.

- □ Support CCIR601/CCIR656 digital video output
- □ Support CCIR601 digital video input

■ Graphic-based OSD
- □ 8-bit OSD architecture
- □ 256 colors simultaneously out of true colors
- □ 8 levels of opacity
- □ Programmable width & height to meet LCD resolution exactly

■ HW audio codec
- □ Integrated 16-bit ADC for mono audio recording
- □ Integrated 16-bit DAC for mono audio playback
- □ Programmable ALC / Noise Gate functions
- □ On-chip pre-amplifier for microphone input
- □ On-chip speaker driver

■ Storage interface
- □ Secure Digital (SD) card
- □ MultiMediaCard (MMC)
- □ SLC NAND type flash
- □ SPI flash

■ USB device controller with built-in transceiver
- □ Fully compliant with USB2.0
- □ High speed (480Mbps) supported
- □ Optionally switchable to be fully compliant with USB1.1
- □ Support PC camera mode
- □ Support charging port detection

■ Timers
- □ RTC can be powered by separate backup battery and operating from 1.2V to 3.6V
- □ Watch dog timer
- □ 8–ch 32-bit timers

■ Peripheral Interface
- □ Support I2C interface
- □ Support flexible PWM interface with DC motor control
- □ Support programmable 3-wired serial interface
- □ Support 2 UART interface
- □ Support 3 channels of 10-bit general purpose ADC

- □ Support multiple input for power button control
- □ Support auto power on system by RTC

■ On-chip boot strap loader

- □ Built-in mask ROM
- □ User programs can be stored in NAND-type flash and external static memory is not necessary
- □ System can boot from internal ROM, SPI flash, NAND flash, SD card and USB
- □ Auto boot mechanism

■ DC/DC converter and Regulator

- □ Built-in 1 buck DC/DC converter for core power
- □ Built-in 2 regulators for sensor power

■ Dual/Triple voltage power supply

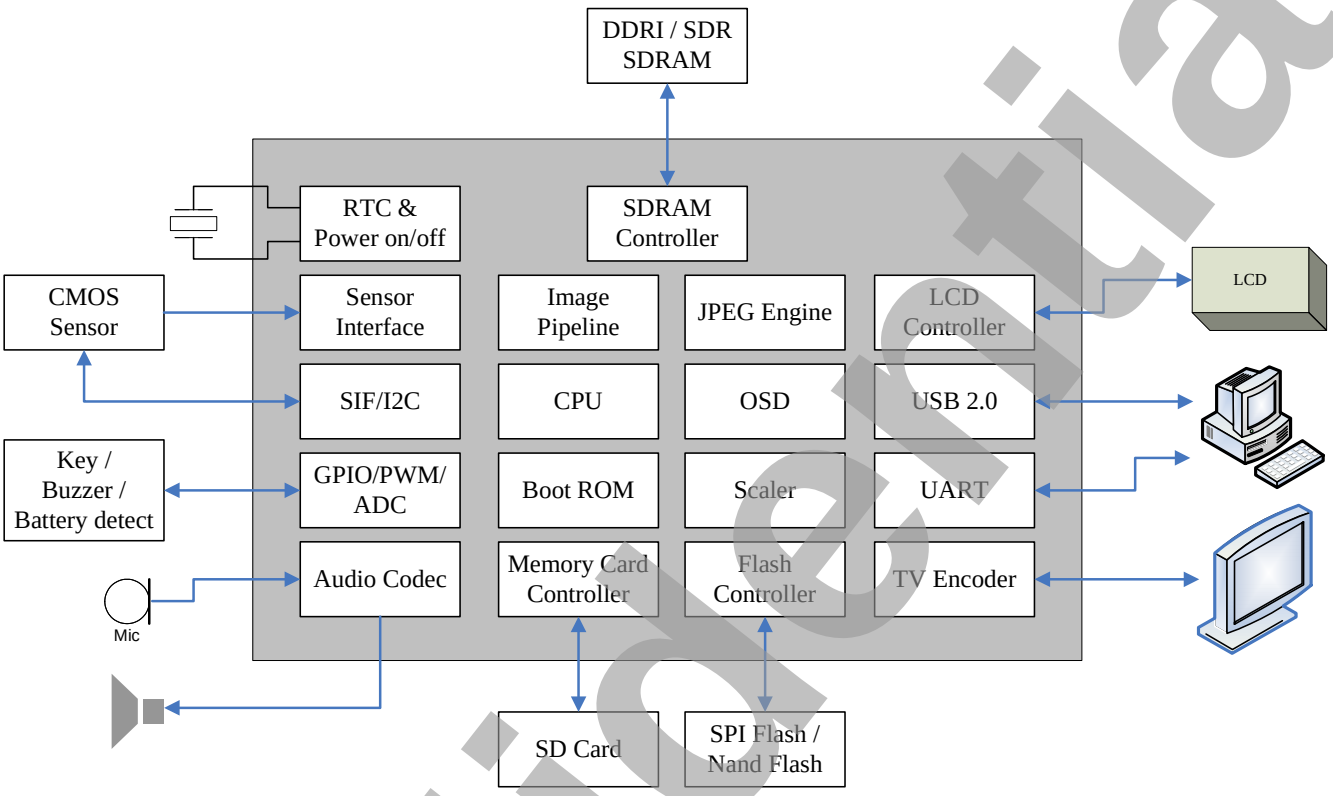
- □ 1.2V core logic voltage
- □ 3.3V SDRAM / 2.5V DDRI SDRAM interface voltage
- □ 3.3V I/O interface and analog circuit voltage

■ NT96223FG 144 TQFP package (16mm x 16mm x 1.1mm)

General Description

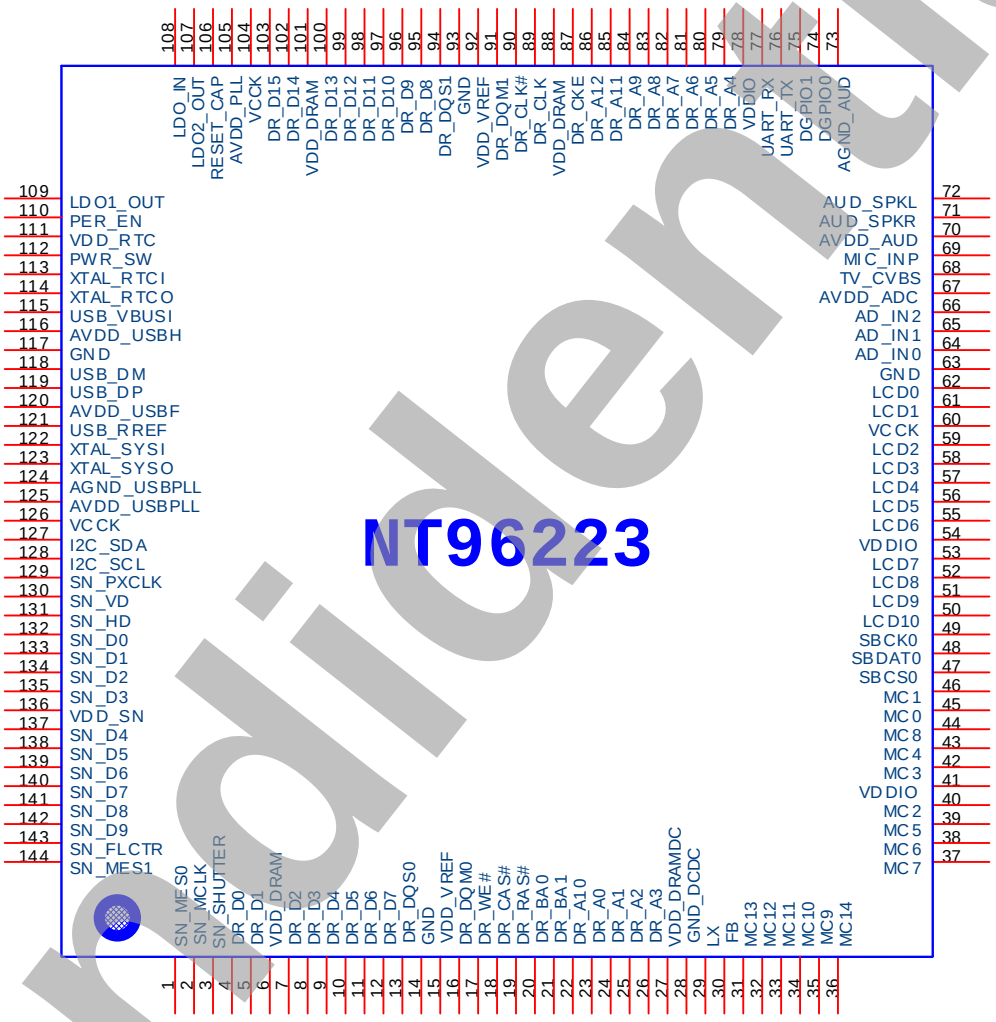
The NT96223FG are high image quality, high performance, and cost effective digital still camera (DSC) /Video Camera recorder (DV) with excellent digital still image capturing and video streaming capabilities. It is targeted at the application of DSC resolutions up to 32M pixels. It can be easily adaptable to many exiting CMOS sensor devices with on chip programmable interface timing approach. The controller provides sophisticated video processing methods with built-in hardware acceleration pipeline. This is essential for achieving high performance for per-shot, shot-to-shot, and continuous shooting pictures. The controller provides flexible mechanism for auto white balance, auto exposure and auto-focusing in order to achieve a better tradeoff for hardware and software efforts over the performance. The interface to SD/MMC, and SMC makes it ideal for the storage of still pictures and video streaming data. The USB2.0 high speed interface can upload/download the video data efficiently to/from PC.

Block Diagram



Pin Configuration

NT96223FG TQFP-144



Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name	Pin No	Pin Name
1	SN_MES0	37	MC7	73	AGND_AUD	109	LDO1_OUT
2	SN_MCLK	38	MC6	74	DGPIO0	110	PWR_EN
3	SN_SHUTTER	39	MC5	75	DGPIO1	111	VDD_RTC
4	DR_D0	40	MC2	76	UART_TX	112	PWR_SW
5	DR_D1	41	VDD_IO	77	UART_RX	113	XTAL_RTCI
6	VDD_DRAM	42	MC3	78	VDD_IO	114	XTAL_RTCO
7	DR_D2	43	MC4	79	DR_A4	115	USB_VBUSI
8	DR_D3	44	MC8	80	DR_A5	116	AVDD_USBHS
9	DR_D4	45	MC0	81	DR_A6	117	GND
10	DR_D5	46	MC1	82	DR_A7	118	USB_DM
11	DR_D6	47	SB_CS0	83	DR_A8	119	USB_DP
12	DR_D7	48	SB_DAT0	84	DR_A9	120	AVDD_USBFS
13	DR_DQS0	49	SB_CK0	85	DR_A11	121	USB_RREF
14	GND	50	LCD10	86	DR_A12	122	XTAL_SYSI
15	VDD_VREF	51	LCD9	87	DR_CKE	123	XTAL_SYSO
16	DR_DQM0	52	LCD8	88	VDD_DRAM	124	AGND_USBPLL
17	DR_WE#	53	LCD7	89	DR_CLK	125	AVDD_USBPLL
18	DR_CAS#	54	VDD_IO	90	DR_CLK#	126	VCCK
19	DR_RAS#	55	LCD6	91	DR_DQM1	127	I2C_SDA
20	DR_BA0	56	LCD5	92	DR_VREF	128	I2C_SCL
21	DR_BA1	57	LCD4	93	GND	129	SN_PXCLK
22	DR_A10	58	LCD3	94	DR_DQS1	130	SN_VD
23	DR_A0	59	LCD2	95	DR_D8	131	SN_HD
24	DR_A1	60	VCCK	96	DR_D9	132	SN_D0
25	DR_A2	61	LCD1	97	DR_D10	133	SN_D1
26	DR_A3	62	LCD0	98	DR_D11	134	SN_D2
27	VDD_DRAMDC	63	GND	99	DR_D12	135	SN_D3
28	GND_DCDC	64	AD_IN0	100	DR_D13	136	VDD_SN
29	LX	65	AD_IN1	101	VDD_DRAM	137	SN_D4
30	FB	66	AD_IN2	102	DR_D14	138	SN_D5
31	MC13	67	AVDD_ADC	103	DR_D15	139	SN_D6
32	MC12	68	TV_CVBS	104	VCCK	140	SN_D7
33	MC11	69	MIV_INP	105	AVDD_PLL	141	SN_D8
34	MC10	70	AVDD_AUD	106	RESET_CAP	142	SN_D9
35	MC9	71	AUD_SPKR	107	LDO2_OUT	143	SN_FLCTR
36	MC14	72	AUD_SPKL	108	LDO_IN	144	SN_MES1

Pin Descriptions

I = input port with Schmitt trigger

O = output port with normal driving/sinking

I/O = bi-directional port with normal driving/sinking and Schmitt input

mvI/O = multi voltage bi-direction port with Schmitt input

I/Ow = bi-directional port with normal driving/sinking and wide Schmitt input range

I/Os = bi-directional port with strong driving/sinking and Schmitt input

I/O_{5VT} = bi-directional port with normal driving/sinking and Schmitt input

OD = open drain output with normal sinking

I/OD = bi-directional port, open drain output with normal sinking and Schmitt input

LVD = low voltage detect function pin

p/u = internal pull-up

p/d = internal pull-down

AI = analog input port

AI_{5VT} = analog 5V tolerant input port

AO = analog output port

AI/O = analog bi-directional port

H = output high

L = output low

P = power or ground

Note: * means this pin has interrupted function.

NT96223FG 144 pins

Total: 144 pins

Alternative GPIO: total 53 pins

System interface (3)

Pin No.	Name	Type	Reset	Descriptions
122	XTAL_SYSI	AI	AI	System clock input. Connect to 12MHz crystal.
123	XTAL_SYSO	AO	AO	System clock output. Connect to 12MHz crystal.
106	RESET_CAP	LVD	-	System Reset Time Capacitor. Connect to capacitor for reset time control.

RTC & Power Button Controller (4)

Pin No.	Name	Type	Reset	Descriptions
113	XTAL_RTCI	AI	-	Real time clock input. Connect to 32768Hz crystal.
114	XTAL_RTCO	AO	-	Real time clock output. Connect to 32768Hz crystal.
112	PWR_SW	AI	I p/d	Power on/off signal input.
110	PWR_EN	AO	-	Power switch or power IC enable signal output.

* PWR_SW can trigger interrupt (share RTC interrupt). If this pin isn't used, Novatek recommends connecting this pin to GND.

DRAM interface (43)

Pin No.	Name	Type	Reset	Descriptions
89	DR_CLK	O	-	DRAM differential clock output
90	DR_CLK#	O	-	
87	DR_CKE	O	-	DRAM clock enable
18	DR_CAS#	O	-	DRAM control signals
19	DR_RAS#			
17	DR_WE#			
15, 92	DR_VREF	AI	-	DDR reference voltage input.(DDR DRAM use only)
20	DR_BA0	O	-	DRAM bank select
21	DR_BA1			
23	DR_A0 / KEY_IN0	I/O	-	DRAM address bus. DR_A0~DR_A6(DR_A5 can not be key sacn input), DR_A7~DR_A12 can be key scan input. Please refer to application circuit for detail implementation. DR_A5 can trigger the test function at reset rising edge
24	DR_A1 / KEY_IN1			
25	DR_A2 / KEY_IN2			
26	DR_A3 / KEY_IN3			
79	DR_A4 / KEY_IN4			
80	DR_A5 / TESTEN			

81	DR_A6 / KEY_IN6			
82	DR_A7 / KEY_IN7			
83	DR_A8 / KEY_IN8			
84	DR_A9 / KEY_IN9			
22	DR_A10 / KEY_IN10			
85	DR_A11 / KEY_IN11			
86	DR_A12 / KEY_IN12			
16	DR_DQM0	O	-	DRAM data mask: DQM0 corresponds to DQ0-DQ7 and DQM1 corresponds to DQ8-DQ15.
91	DR_DQM1			
13	DR_DQS0	I/O	-	DRAM data strobe. DQS0 corresponds to DQ0-DQ7 and DQS1 corresponds to DQ8-DQ15.
94	DR_DQS1			
4	DR_D0	I/O	-	DRAM Data input/output
5	DR_D1			
7	DR_D2			
8	DR_D3			
9	DR_D4			
10	DR_D5			
11	DR_D6			
12	DR_D7			
95	DR_D8			
96	DR_D9			
97	DR_D10			
98	DR_D11			
99	DR_D12			
100	DR_D13			
102	DR_D14			
103	DR_D15			

Sensor interface (20)

Pin No.	Name	Type	Reset	Descriptions
132	SN_D0 / SGPIO0*	mvI/O	I p/d	Sensor data input
133	SN_D1 / SGPIO1*			
134	SN_D2 / SGPIO2			
135	SN_D3 / SGPIO3			
137	SN_D4 / SGPIO4			

138	SN_D5 / SGPIO5			
139	SN_D6 / SGPIO6			
140	SN_D7 / SGPIO7			
141	SN_D8 / SGPIO8			
142	SN_D9 / SGPIO9			
129	SN_PXCLK / SGPIO10	mvI/Os	I p/d	Sensor Pixel Clock Input
130	SN_VD / SGPIO11	mvI/Os	I p/d	Timing Generator Vertical Sync.
131	SN_HD / SGPIO12	mvI/Os	I p/d	Timing Generator Horizontal Sync.
3	SN_SHUTTER / SGPIO13*	mvI/Os	I p/d	SHUTTER Control Signal for CMOS sensor
2	SN_MCLK / SGPIO14*	mvI/Os	I p/d	Master Clock to Timing Generator
127	I2CSDA / SGPIO15	mvI/OD	I p/u	I2C Serial Data
128	I2CSCL / SGPIO16	mvI/OD	I p/u	I2C Serial Clock
1	SN_MES0 / SGPIO17*	mvI/Os	I p/d	Mechanical Shutter 0
144	SN_MES1 / SGPIO18*	mvI/Os	I p/d	Mechanical Shutter 1
3	SN_FLCTR / SGPIO19*	mvI/Os	I p/d	Flash Control

Note*: The pin can trigger interrupt.

Note: The mvI/O voltage of Sensor interface corresponds to VDD_SN.

Memory Card interface (15)

Pin No.	Name	Type	Reset	Descriptions
45	MC0 / CGPIO0	I/O	I p/u	Memory Card interface
46	MC1 / CGPIO1	I/O	I p/u	
40	MC2 / CGPIO2	I/Os	I p/u	
42	MC3 / CGPIO3	I/O	I p/u	
43	MC4 / CGPIO4	I/O	I p/u	
39	MC5 /	I/O	I p/d	

	CGPIO5*		
38	MC6 / CGPIO6*	I/O	I p/d
37	MC7 / CGPIO7*	I/O	I p/d
44	MC8 / CGPIO8	I/Os	I p/u
35	MC9 / CGPIO9*	I/O	I p/u
34	MC10 / CGPIO10*	I/O	I p/u
33	MC11 / CGPIO11*	I/Os	I p/d
32	MC12 / CGPIO12*	I/O	I p/d
31	MC13 / CGPIO13*	I/O	I p/u
36	MC14 / CGPIO14	I/O	I p/u

Note*: The pin can trigger interrupt.

Memory card interface pinmux table

Name	NAND Flash		SD/MMC		Serial Flash		Serial(4)Flash		i-80 CSTN	
MC0	NAND_D0	I/O	SD_D0	I/O	SPI_DO	O	SPI_D0	I/O		
MC1	NAND_D1	I/O	SD_D1	I/O	SPI_DI	I	SPI_D1	I/O		
MC2	NAND_D2	I/O	SD_D2	I/O	SPI_CLK	O	SPI_CLK	O		
MC3	NAND_D3	I/O	SD_D3	I/O			SPI_D2	I/O		
MC4	NAND_D4	I/O	SD_CMD	I/O			SPI_D3	I/O		
MC5	NAND_D5	I/O							CSTN_TE	I
MC6	NAND_D6	I/O							CSTN_SDI	I
MC7	NAND_D7	I/O							CSTN_SDO	O
MC8		O	SD_CLK	O						
MC9	NAND_WE#	O	SD_D4	I/O					CSTN_SDIO	I/O
MC10	NAND_RE#	O	SD_D5	I/O					CSTN_SSEL	O
MC11	NAND_CLE	O	SD_D6	I/O					CSTN_SCLK	O
MC12	NAND_ALE	O	SD_D7	I/O						
MC13	NAND_RDY	I							CSTN_SCS	O
MC14	NAND_CS	O			SPI_CS#	O	SPI_CS#	O		

LCD interface (11)

Pin No.	Name	Type	Reset	Descriptions
62	LCD0 / LGPIO[0] / BS0	I/O	I p/d	LCD Signal Bus / BS2..0: Boot source selection The boot source setting description: 0x0: Auto boot select (SPI -> USB full -> SDIO) 0x1: Serial Flash (SPI) 3 byte 0x2: SDIO 0x3: NAND with Hamming ECC 0x4: USB auto speed detect 0x5: USB force full speed 0x6: Auto boot select (NAND -> USB full -> SDIO) 0x7: NAND without ECC
61	LCD1 / LGPIO[1] / BS1	I/O	I p/d	
59	LCD2 / LGPIO[2] / BS2	I/O	I p/d	

58	LCD3 / LGPIO[3] / BS3	I/O	I p/d	LCD Signal Bus BS6..3 is for IC debugging setting. Please keep low at reset signal rising edge.
57	LCD4 / LGPIO[4] / BS4	I/O	I p/d	
56	LCD5 / LGPIO[5] / BS5	I/O	I p/d	
55	LCD6 / LGPIO[6] / BS6	I/O	I p/d	
53	LCD7 / LGPIO[7]	I/O	I p/d	LCD Signal Bus
52	LCD8 / LGPIO[8]	I/Os	I p/d	
51	LCD9 / LGPIO[9]	I/O	I p/d	
50	LCD10 / LGPIO[10]	I/Os	I p/d	

LCD interface pinmux table

Name	Bootstrap	CCIR656		CCIR601		Serial RGB		CSTN/Parallel		CSTN/Serial	
LCD0	BS0	YC0	O	YC0	O	D0	O	CSTNP_DO	I/O		
LCD1	BS1	YC1	O	YC1	O	D1	O	CSTNP_D1	I/O		
LCD2	BS2	YC2	O	YC2	O	D2	O	CSTNP_D2	I/O		
LCD3	BS3	YC3	O	YC3	O	D3	O	CSTNP_D3	I/O		
LCD4	BS4	YC3	O	YC3	O	D4	O	CSTNP_D4	I/O	CSTNS_TE	I
LCD5	BS5	YC5	O	YC5	O	D5	O	CSTNP_D5	I/O	CSTNS_DI	I
LCD6	BS6	YC6	O	YC6	O	D6	O	CSTNP_D6	I/O	CSTNS_DO	O
LCD7		YC7	O	YC7	O	D7	O	CSTNP_D7	I/O	CSTNS_DIO	I/O
LCD8		CLK	O	CLK	O	CLK	O	CSTNP_CS	O	CSTNS_CS	O
LCD9				VS	O	VS	O	CSTNP_SEL	O	CSTNS_SEL	O
LCD10				HS	O	HS	O	CSTNP_WR	O	CSTNS_CLK	O
SBCK0								CSTNP_RD	O		
SBDAT0								CSTNP_D8	I/O		
SBCS0								CSTNP_TE	O		

Peripheral I/O (7)

Pin No.	Name	Type	Reset	Descriptions
49	SBCK0 / PGPIO0	I/O	I p/d	Serial Interface Clock 0
48	SBDAT0 / PGPIO1	I/O	I p/d	Serial Interface Data 0
47	SBCS0 / PGPIO2	I/O	I p/u	Serial Interface Chip Enable 0
76	UART_TX / PGPIO7	I/O	I p/u	UART Transmit
77	UART_RX /	I/O	I p/u	UART Receive

	PGPIO8			
74	DGPIO0*/ PI_CNT	I/Osw	I p/d	General purpose input/output pin
75	DGPIO1*	I/Osw	I p/d	General purpose input/output pin

Peripheral pinmux table

Name	PWM		UART2		Alternate Function 1		Alternate Function 2	
DGPIO0			UART2_TX	O	PWM1	O	PI_CNT	I
DGPIO1			UART2_RX	I				

ADC interface (3)

Pin No.	Name	Type	Reset	Descriptions
64	AD_IN0	AI	-	General ADC Input
65	AD_IN1	AI	-	General ADC Input
66	AD_IN2	AI	-	General ADC Input

TV interface (1)

Pin No.	Name	Type	Reset	Descriptions
68	TV_CVBS	AO	-	Video Data Output Composite video output

Audio (3)

Pin No.	Name	Type	Reset	Descriptions
69	MIC_INP	AI	-	Microphone Input
71	AUD_SPKR	AO	-	Speaker Output of Right Channel
72	AUD_SPKL	AO	-	Speaker Output of Left Channel (or Line out)

USB device interface (4)

Pin No.	Name	Type	Reset	Descriptions
115	USB_VBUSI*	AI_{5VT}	-	USB V_{BUS} Input. This pin is 5V tolerance input
119	USB_DP	AI/O	-	USB FS/HS Differential Data Plus (D+)
118	USB_DM	AI/O	-	USB FS/HS Differential Data Minus (D-)
121	USB_RREF	AI	-	USB reference resistor. Connect 2KΩ/1% resistor to GND

DC/DC conveter and Regulator (5)

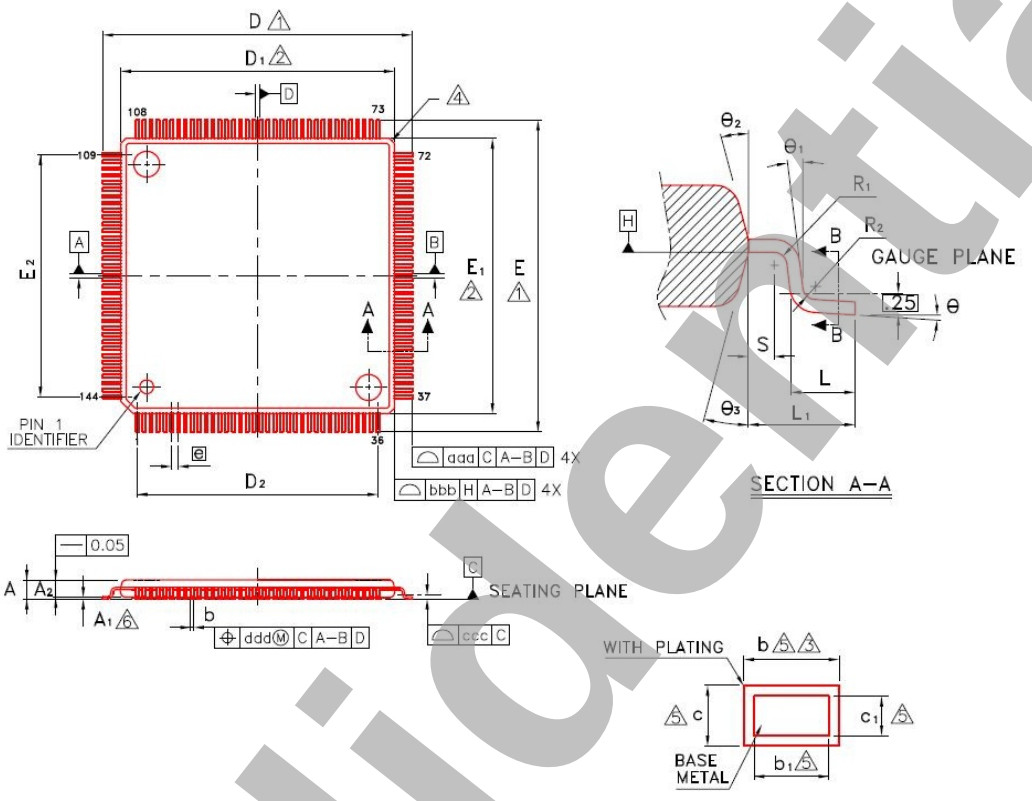
Pin No.	**Name**	**Type**	**Reset**	**Descriptions**
29	LX	AO	-	Switching pin of DC/DC converter
30	FB	AI	-	Feedback pin of DC/DC converter
108	LDO_IN	P	-	Regulator Input
109	LDO_OUT1	P	-	Regulator Output 1
107	LDO_OUT2	P	-	Regulator Output 2

Power (25)

Pin No.	Name	Type	Descriptions
60, 104, 126	VCCK	P	Core Power
41, 54, 78	VDD_IO	P	I/O Pad Power
14, 63, 93, 117	GND	P	Digital Ground
6, 88, 101	VDD_DRAM	P	DRAM I/O power. (3.3V for SDR; 2.5V for DDR1.)
27	VDD_DRAMDC	P	DCDC & DRAM I/O power. (3.3V for SDR; 2.5V for DDR1.)
28	GND_DCDC	P	DC/DC converter Ground
136	VDD_SN	P	Sensor multi-level IO Power
111	VDD_RTC	P	RTC Power
116	AVDD_USBHS	P	USB High Speed Transceiver Power
124	AGND_USBPLL	P	USB PLL Ground
120	AVDD_USBFS	P	USB Full Speed Transceiver Power
67	AVDD_ADC	P	3.3V ADC Power
70	AVDD_AUD	P	Audio Codec Power
73	AGND_AUD	P	Audio Codec Ground
125	AVDD_USBPLL	P	USB PLL analog Power
105	AVDD_PLL	P	PLL analog Power

Package Outline

TQFP-144



NOTE :

1. TO BE DETERMINED AT SEATING PLANE C .
2. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR CAN NOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.
4. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
5. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm AND 0.25 mm FROM THE LEAD TIP.
6. A1 IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. CONTROLLING DIMENSION : MILLIMETER.

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	1.00	1.10	1.20	0.039	0.043	0.047
A_1	0.05	0.10	0.15	0.002	0.004	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.13	0.18	0.23	0.005	0.007	0.009
b_1	0.13	0.16	0.19	0.005	0.006	0.007
c	0.09	—	0.20	0.004	—	0.008
c_1	0.09	—	0.16	0.004	—	0.006
D	18.00 BSC			0.709 BSC		
D_1	16.00 BSC			0.630 BSC		
D_2	14.00 BSC			0.551 BSC		
E	18.00 BSC			0.709 BSC		
E_1	16.00 BSC			0.630 BSC		
E_2	14.00 BSC			0.551 BSC		
e	0.40 BSC			0.016 BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L_1	1.00 REF			0.039 REF		
R_1	0.08	—	—	0.003	—	—
R_2	0.08	—	0.20	0.003	—	0.008
S	0.20	—	—	0.008	—	—
θ	0°	3.5°	7°	0°	3.5°	7°
$θ_1$	0°	—	—	0°	—	—
$θ_2$	11°	12°	13°	11°	12°	13°
$θ_3$	11°	12°	13°	11°	12°	13°
aaa	0.20			0.008		
bbb	0.20			0.008		
ccc	0.08			0.003		
ddd	0.07			0.003		

Electrical Characteristics

Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Supply Voltage of 1.2V Core power	V_{CCK}	-0.3 ~ +1.4	V
Supply Voltage of 3.3V Digital I/O	V_{DD_IO}, V_{DD_DRAM}, V_{DD_SN}, V_{DD_RTC}	-0.3 ~ +3.8	V
Supply Voltage of 1.2V analog block	AV_{DD_USBHS}, AV_{DD_USBPLL}, AV_{DD_HDM}, AV_{DD_PLL}	-0.3 ~ +1.4	V
Supply Voltage of 3.3V analog block	AV_{DD_USBFS}, AV_{DD_ADC}, AV_{DD_DAC}, AV_{DD_AUD}	-0.3 ~ +3.8	V
Input/Output Voltage	I/O	-0.3 ~ V_{DD_IO} +0.3	V
Input Voltage(5V Tolerant)	I/O_{5VT}	-0.3 ~ +5.8	V
Operating Ambient Temperature	T_{OPR}	-10 ~ 70	^{0}C
Storage Temperature	T_{STG}	-55 ~ 125	^{0}C

Comment

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

ESD performance

Model	Standard	Classification	Note
Human Body Mode(HBM)	MIL-STD-883G Method 3015.7	Class : 2	2K~3KV
Machine Mode(MM)	JEDEC Specification EIA/JESD22-A115	Class : B	200~400V
CDM Mode(CDM)	JEDEC Specification JESD22-C101		

Latch-up Immunity

Model	Standard	Classification	Note
Latch up	JEDEC Specification JESD-78A	Class : I	±200mA

Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{CCK}	Core Logic Operating Voltage	1.08	1.2	1.32	V	

V_{DD_IO}	General I/O Interface Operating Voltage	3.0	3.3	3.6	V	
V_{DD_DRAM}	DDR DRAM Interface Operating Voltage	3.0	3.3	3.6	V	SDRAM
V_{DD_DRAM}	SDRAM I/O Interface Operating Voltage	2.3	2.5	2.7	V	DDR DRAM
V_{DD_SN}	I/O of Sensor Interface Operating Voltage	1.62	3.3	3.6	V	1.8V~3.3V
V_{DD_RTC}	RTC Operating Voltage	1.5	3.3	3.6	V	
AV_{DD_USBHS}	USB High Speed Transceiver Operating Voltage	1.08	1.2	1.32	V	
AV_{DD_USBPLL}	PLL of USB Transceiver Operating Voltage	1.08	1.2	1.32	V	
AV_{DD_USBFS}	USB Full Speed Transceiver Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_ADC}	ADC Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_DAC}	Video DAC Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_AUD}	Audio Code and Speaker Amplifier Operating Voltage	3.0	3.3	3.6	V	
AV_{DD_HDMI}	HDMI Transceiver Operating Voltage	1.08	1.2	1.32	V	
AV_{DD_PLL1}	PLL1 Operating voltage	1.08	1.2	1.32	V	
AV_{DD_PLL2}	PLL2 Operating voltage	1.08	1.2	1.32	V	

DC Characteristics

General I/O

(V_{CCK}=1.2V, Temp=25^{0}C)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
P_{RUN}	Operating Power Consumption	-	260	-	mW	720p30
I_{RTC}	Operation current of RTC	-	5	-	uA	V_{DD_RTC} = 3.3V
I/O General characteristic						
V_{IH}	Input High Voltage (I/O)	2.0	-	-	V	IO voltage @ 3.3V / 2.5V / 1.8V
		1.7	-	-	V	
		1.2	-	-	V	
V_{IL}	Input Low Voltage (I/O)	-	-	0.8	V	IO voltage @ 3.3V / 2.5V / 1.8V
		-	-	0.7	V	
		-	-	0.6	V	
V_{T+}	Schmitt Trigger Positive Going Threshold (I/O)	-	1.7	2.0	V	IO voltage @ 3.3V / 2.5V / 1.8V
		-	1.34	1.7	V	
		-	1.05	1.2	V	
V_{T-}	Schmitt Trigger Negative Going Threshold (I/O)	0.8	1.4	-	V	IO voltage @ 3.3V / 2.5V / 1.8V
		0.7	1.07	-	V	
		0.6	0.76	-	V	
I_{OH}	Output Driving Current (IO voltage @ 3.3V)	2.5	-	-	mA	V_{OH}=V_{DD}-0.4V, @ 2.5 / 5 / 7.5 / 10 mA setting
		5	-	-	mA	
		7.5	-	-	mA	
		10	-	-	mA	
I_{OL}	Output Sinking Current (IO voltage @ 3.3V)	2.5	-	-	mA	V_{OL}=GND+0.4V, @ 2.5 / 5 / 7.5 / 10 mA setting
		5	-	-	mA	
		7.5	-	-	mA	
		10	-	-	mA	
I_{OH}	Output Driving Current (IO voltage @ 2.5V)	2	-	-	mA	V_{OH}=V_{DD}-0.4V, @ 2.5 / 5 / 7.5 / 10 mA setting
		4	-	-	mA	
		6	-	-	mA	
		8	-	-	mA	
I_{OL}	Output Sinking Current (IO voltage @ 2.5V)	2	-	-	mA	V_{OL}=GND+0.4V, @ 2.5 / 5 / 7.5 / 10 mA setting
		4	-	-	mA	
		6	-	-	mA	
		8	-	-	mA	
I_{OH}	Output Driving Current (IO voltage @ 1.8V)	1.5	-	-	mA	V_{OH}=V_{DD}-0.4V, @ 2.5 / 5 / 7.5 / 10 mA setting
		3	-	-	mA	
		4.5	-	-	mA	
		6	-	-	mA	
I_{OL}	Output Sinking Current (IO voltage @ 1.8V)	1.5	-	-	mA	V_{OL}=GND+0.4V, @ 2.5 / 5 / 7.5 / 10 mA setting
		3	-	-	mA	
		4.5	-	-	mA	
		6	-	-	mA	
$I_{IL\,eakage}$	Input Leakage Current	-	±1	±10	uA	GND≤V_{IN}≤V_{DD}, input w/o R_{PU}/R_{PD}
R_{PU}	Internal Pull-up Resistor	26	36	65	KΩ	V_{IN}=V_{DD},

		33	48	93	KΩ	I/O power @ 3.3 / 2.5 / 1.8 V
		-	78	-	KΩ	
R_{PD}	Internal Pull-down Resistor	26	36	65	KΩ	V_{IN}=GND, I/O power @ 3.3 / 2.5 / 1.8 V
		33	48	93	KΩ	
		-	78	-	KΩ	
I/Ow (wide Schmitt input range)						
V_{T+}	Schmitt Trigger Positive Going Threshold (I/Ow)	-	1.7	2.0	V	IO voltage @ 3.3V
V_{T-}	Schmitt Trigger Negative Going Threshold (I/Ow)	0.8	1.1	-	V	
I/O_{5VT} (5V tolerance I/O Schmitt input range)						
V_{T+}	Schmitt Trigger Positive Going Threshold (I/O_{5VT})	-	1.7	2.0	V	IO voltage @ 3.3V
V_{T-}	Schmitt Trigger Negative Going Threshold (I/O_{5VT})	1.0	1.40	-	V	
I/O_s (strong driving/sinking output capacity)						
I_{OH}	Output Driving Current (IO voltage @ 3.3V)	5	-	-	mA	V_{OH}=V_{DD}-0.4V, @ 5 / 10 / 15 / 20 mA setting
		10	-	-	mA	
		15	-	-	mA	
		20	-	-	mA	
I_{OL}	Output Driving Current (IO voltage @ 3.3V)	5	-	-	mA	V_{OL}=GND+0.4V, @ 5 / 10 / 15 / 20 mA setting
		10	-	-	mA	
		15	-	-	mA	
		20	-	-	mA	
I_{OH}	Output Driving Current (IO voltage @ 2.5V)	4	-	-	mA	V_{OH}=V_{DD}-0.4V, @ 5 / 10 / 15 / 20 mA setting
		8	-	-	mA	
		12	-	-	mA	
		16	-	-	mA	
I_{OL}	Output Driving Current (IO voltage @ 2.5V)	4	-	-	mA	V_{OL}=GND+0.4V, @ 5 / 10 / 15 / 20 mA setting
		8	-	-	mA	
		12	-	-	mA	
		16	-	-	mA	
I_{OH}	Output Sinking Current (IO voltage @ 1.8V)	3	-	-	mA	V_{OH}=V_{DD}-0.4V, @ 5 / 10 / 15 / 20 mA setting
		6	-	-	mA	
		9	-	-	mA	
		12	-	-	mA	
I_{OL}	Output Sinking Current (IO voltage @ 1.8V)	3	-	-	mA	V_{OL}=GND+0.4V, @ 5 / 10 / 15 / 20 mA setting
		6	-	-	mA	
		9	-	-	mA	
		12	-	-	mA	

Specific function I/O

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RESET_CAP & Low Voltage Detector						
R_{PU}	Pull-Up Resistor of RESET_CAP	80	100	130	KΩ	V_{DD}=3.3V

$R_{DS(ON)\_LVD}$	RDS of LVD active	200	800	1300	Ω	V_{DD}=2.5V, V_{OL}=GND+0.4V
$V_{IH(DET)}$	Detect Level Vih	-	2.65	2.9	V	
$V_{IL(DET)}$	Detect Level Vil	2.25	2.55	-	V	
$V_{H(LVD)}$	Hysteresis Voltage	-	100	-	mV	
Power Button Controller						
R_{PD}	Pull-Down Resistor (PWR_SW)	170	270	450	KΩ	
V_{T+}	Schmitt Trigger Positive Going Threshold (PWR_SW)	-	1.0	1.2	mV	V_{DD_RTC}=3.3V
V_{T-}	Schmitt Trigger Negative Going Threshold (PWR_SW)	0.7	0.9	-	mV	V_{DD_RTC}=3.3V
R_{PD}	Pull-Down Resistor (USB_VBUSI)	0.5	1.0	2.4	MΩ	
V_{IH}	Input High Voltage (USB_VBUSI)		1.65	1.85	V	V_{DD_RTC}=3.3V
V_{IL}	Input Low Voltage (USB_VBUSI)	0.95	1.1		V	V_{DD_RTC}=3.3V
R_{OH}	Resistor of PWR_EN Output High	1100	1300	1500	Ω	V_{OH}=2.9V, V_{DD_RTC}=3.3V
R_{OL}	Resistor of PWR_EN Output Low	180	250	220	Ω	V_{OL}=0.4V, V_{DD_RTC}=3.3V

DDR DRAM

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD_DRAM}	DRAM I/O Supply Voltage	2.3	2.5	2.7	V	
V_{REF}	DRAM I/O Reference Voltage	0.49 * VDDQ	1.25	0.51 * VDDQ	V	
$V_{IH(DC)}$	DRAM I/O DC Input High (Logic 1) Voltage	V_{REF} +0.15	-	V_{DD} +0.3	V	
$V_{IL(DC)}$	DRAM I/O DC Input Low (Logic 0) Voltage	-0.3	-	V_{REF} -0.15	V	
$V_{IH(AC)}$	DRAM I/O AC Input High (Logic 1) Voltage	V_{REF} +0.31	-	V_{DD} +0.3	V	
$V_{IL(AC)}$	DRAM I/O AC Input Low (Logic 0) Voltage	-0.3	-	V_{REF} -0.31	V	
I_{OH}	DRAM I/O Output Driving Current	-	2~18	-	mA	V_{OH}=2.15V, 8 steps adjustable
I_{OL}	DRAM I/O Output Sinking Current	-	2~18	-	mA	V_{OL}=0.35V, 8 steps adjustable
$I_{ILeakage}$	Input Leakage Current	-	±1	±10	uA	GND≤V_{IN}≤V_{DD}, input w/o R_{PD}
R_{PD}	Internal Pull-down Resistor	75	150	220	KΩ	V_{IN}≤V_{DD}, V_{DD_DRAM} = 2.5V

SDRAM

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD_DRAM}	DRAM I/O Supply Voltage	3.0	3.3	3.6	V	
V_{IH}	DRAM I/O DC Input High (Logic 1) Voltage	2.0	-	V_{DD} +0.3	V	
V_{IL}	DRAM I/O DC Input Low (Logic 0) Voltage	-0.3	-	0.8	V	
I_{OH}	DRAM I/O Output Driving Current	-	2.5~20	-	mA	V_{OH}=2.9V, 8 steps adjustable
I_{OL}	DRAM I/O Output Sinking Current	-	2.5~20	-	mA	V_{OL}=0.4V, 8 steps adjustable
$I_{ILeakage}$	Input Leakage Current	-	±1	±10	uA	GND≤V_{IN}≤V_{DD}, Pin is input state
R_{PD}	Internal Pull-down Resistor	50	100	150	KΩ	V_{IN}≤V_{DD}, V_{DD_DRAM} = 3.3V

USB

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
High Speed Transceiver						
Input Levels (differential receiver)						
V_{HSDIFF}	High speed differential input sensitivity	300	-	-	mV	$\|V_{I(DP)}-V_{I(DM)}\|$ measured at the connection as application circuit
V_{HSCM}	High speed data signaling common mode voltage range	-50	-	500	mV	
V_{HSSQ}	High speed squelch detection threshold	-	-	100	mV	squelch detected
		150	-	-	mV	no squelch detected
V_{HSDSC}	High speed disconnection detection threshold	625	-	-	mV	disconnection detected
		-	-	525	mV	disconnection not detected
Output Levels						
V_{HSOI}	High speed idle level output voltage (differential)	-10	-	10	mV	
V_{HSOL}	High speed low level output voltage (differential)	-10	-	10	mV	
V_{HSOH}	High speed high level output voltage (differential)	-360	-	400	mV	
V_{CHRPJ}	Chirp-J output voltage (differential)	700	-	1100	mV	
V_{CHIRPK}	Chirp-K output voltage (differential)	-900	-	-500	mV	
Resistance						
R_{DRV}	Driver output impedance	3	6	9	Ω	equivalent resistance used as internal chip only
		40.5	45	49.5	Ω	overall resistance including external resistor

Termination						
V_{TERM}	Termination voltage for pull-up resistor on pin RPU	3.0	-	3.6	V	
Full / Low Speed Transceiver						
Input Levels (differential receiver)						
V_{DI}	Differential input sensitivity	0.2	-	-	V	$\|V_{I(DP)}-V_{I(DM)}\|$
V_{CM}	Differential common mode voltage	0.8	-	2.5	V	
Input Levels (single-ended receivers)						
V_{SE}	Single ended receiver threshold	0.8	-	2.0	V	
Output Levels						
V_{OL}	Low-level output voltage	0	-	0.3	V	
V_{OH}	High-level output voltage	2.8	-	3.6	V	

Buck DC/DC converter

(V_{IN} = 2.5V, Temp=25^{0}C)

Symbol	Parameter	Min.	Typical	Max.	Unit	Conditions
V_{IN}	Input Voltage Range	2.3	2.5	3.60	V	DDR Vin=2.5V;SDR Vin=3.3V
ΔV_{OUT}	Output Voltage Accuracy	-10	-	+10	%	Iout = 100mA
$R_{DS(ON)\_P}$	R_{ON} of P-MOSFET	-	-	1.4	Ω	Open loop Iout=100mA
$R_{DS(ON)\_N}$	R_{ON} of N-MOSFET	-	-	1.1	Ω	Open loop Iout=100mA
F_{OSC}	Oscillator Frequency	1.1	-	2.0	MHz	
I_{FB}	FB pin input current	-	<0.1	-	uA	
I_{LM}	Current Limit	-	175	-	mA	Peak current
D_{MAX}	Max. Duty Cycle	-	100	-	%	
Eff	DC/DC Efficiency	85	-	-	%	Vin=3.3V;Iout=110mA; L=4.7uH

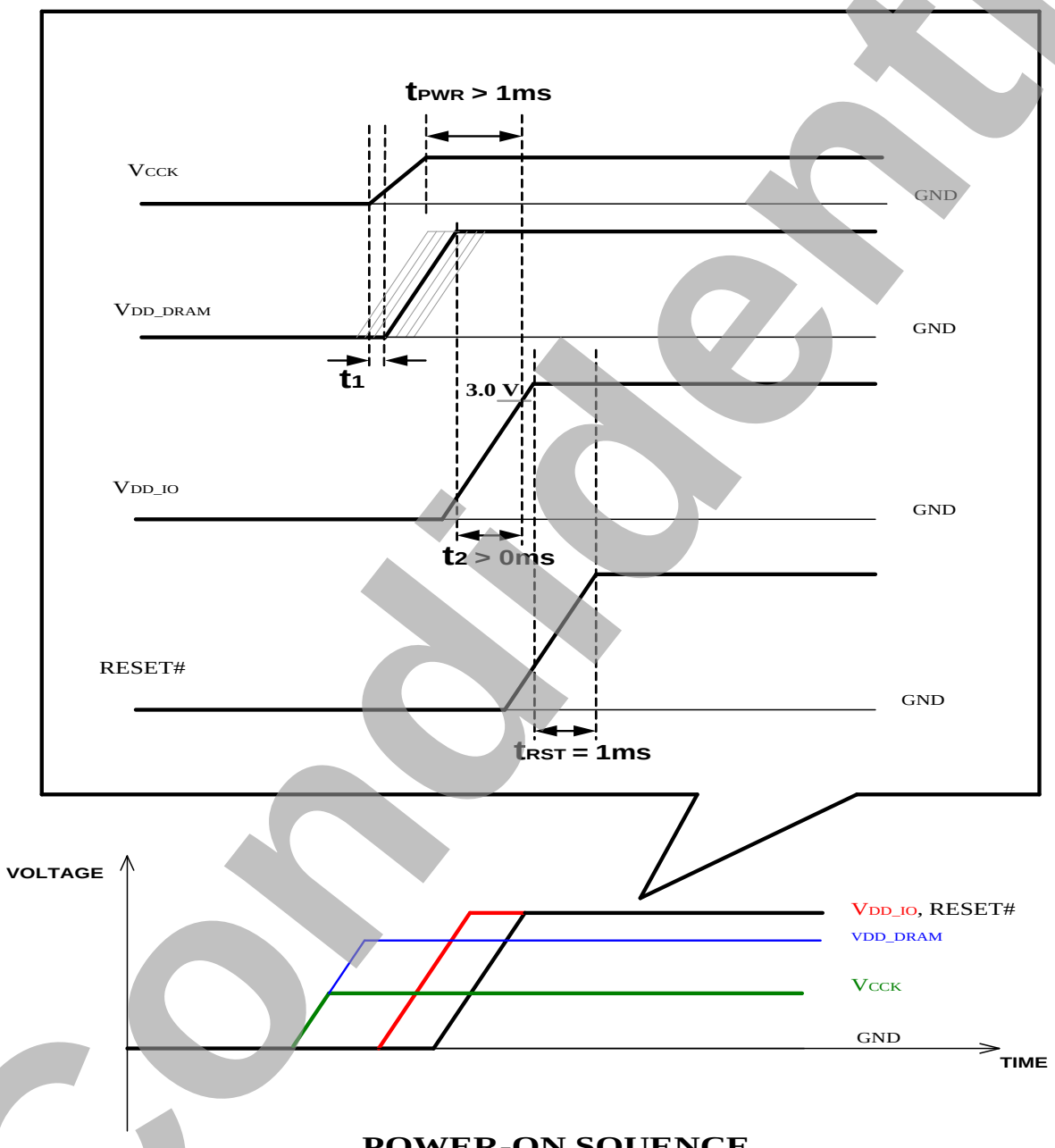
LDO Electrical Characteristics

Symbol	Parameter	Min.	Typical	Max.	Unit	Conditions
V_{IN}	Input Voltage Range	3.0	3.3	3.6	V	
ΔV_{OUT}	Output Voltage Accuracy	-10	-	+10	%	IOUT = 100mA
V_{DROP}	Dropout voltage	-	60	65	mV	IOUT = 100mA Vout=2.8V
		-	50	55	mV	IOUT = 60mA Vout=2.8V

I_Q	Quiescent Current	-	320	450	uA	VIN = 3.3V, Iout=0mA
I_{STBY}	Shutdown Current	-	0.01	1	uA	Disable LDO
I_{Max}	Maximum Output Current	-	-	100	mA	
ΔV_{LOAD}	Load Regulation	-	3.5	-	%	Vin=3.3V,output1.2mA to 100mA

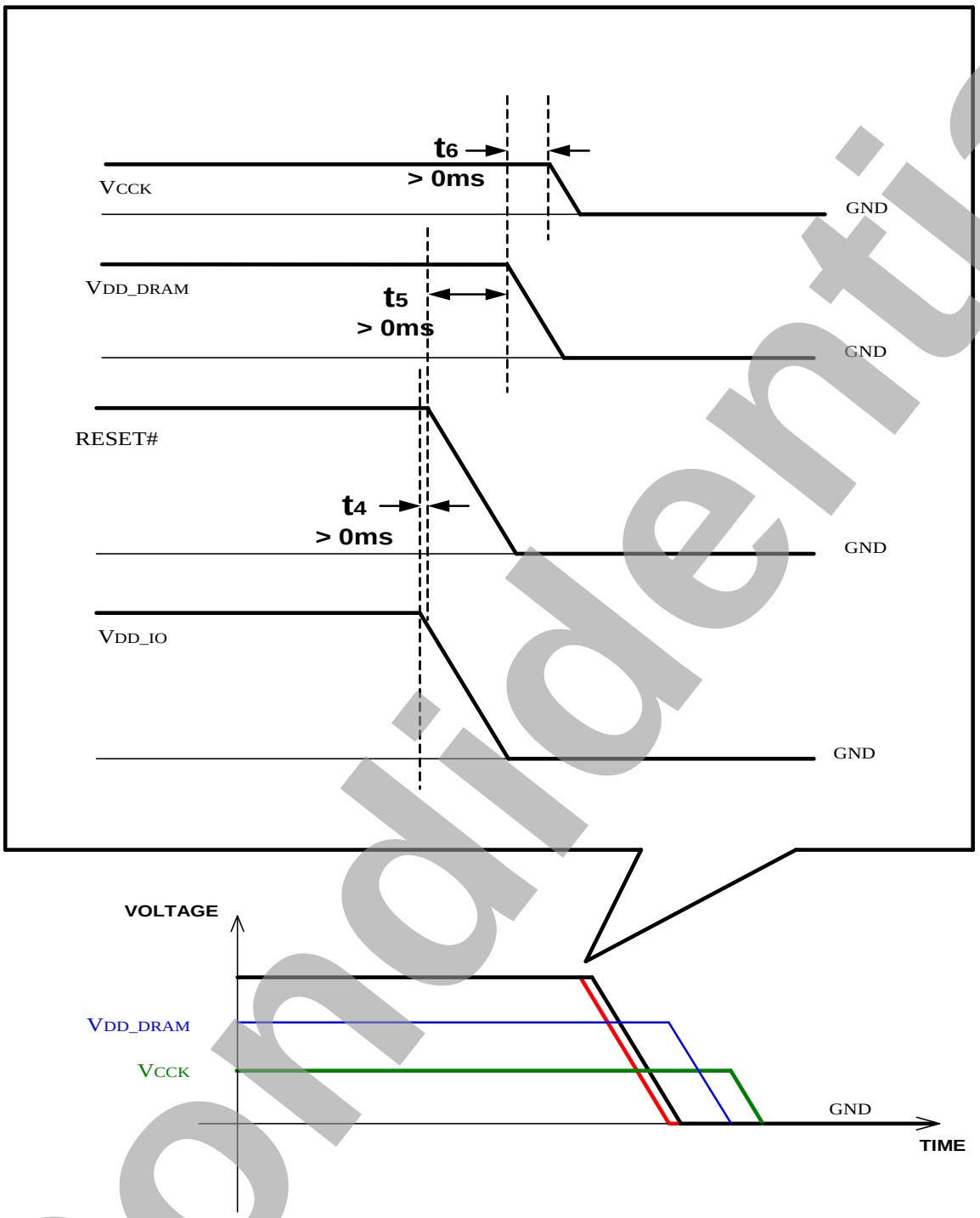
AC Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
T_{RTC}	RTC 32768Hz crystal warm up time	-	500	800	ms	V_{DD_RTC}=3V
t_{RST}	RESET# sustained time	1	-	-	ms	after power being stable
t_{PWR}	Core power prior to I/O power time	1	-	-	ms	



POWER-ON SQUENCE

Note : Even $t_1 \geqq 0$ ms or $t_1 < 0$ ms is acceptable, but it is necessary to make sure $t_2 > 0$ ms .



POWER-OFF SEQUENCE

Note：

Novatek recommends that $t_4 > 0$ ms, $t_5 > 0$ ms, and $t_6 > 0$ ms for a stable system application. But they are not the required restrictions for Novatek's DSP.

ADC

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{DD_ADC}	Supply Voltage	3.0	3.3	3.6	V	
RES	ADC Effective Resolution	-	8	-	Bits	10 bits SAR ADC
V_{Input}	AD_IN1 Input signal level	0.6	-	V_{DD_ADC}	V	
V_{Input}	AD_IN2/3 Input signal level	0	-	V_{DD_ADC}	V	
INL	Integral nonlinearity	-	±1	-	LSB	
DNL	Differential nonlinearity	-	±0.5	-	LSB	
C_{IN}	Input capacitance	-	20	-	pF	
I_{DD_ADC}	Operating Current	-	0.2	-	mA	

TV encoder

(Rload = 37.5Ω, Conversion rate = 27MHz)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
RES	Video DAC Effective Resolution	-	8	-	bits	10-Bits I-Steering DAC structure
INL	Integral Nonlinearity, INL	-	±1	-	LSB	
DNL	Differential Nonlinearity, DNL	-	±0.5	-	LSB	
I_{code}	Output Current-DAC Code 1023 (Iout FS)	-	34.08	-	mA	R_{load} = 37.5 Ohm
V_{code}	Out Voltage-DAC Code 1023	-	1.28	-	V	R_{load} = 37.5 Ohm
VLE	Video Level Error	-5	-	+5	%	
V_{oc}	Output Compliance Range	0	-	1.4	V	
F_{clk}	Conversion rate	-	27	-	MHz	

Audio Codec

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Microphone Input						
V_{IN}	Input Full Scale Level	-	1	-	Vpp	0dB gain
SNR	Signal to Noise Ratio	-	67	-	dBA	0dB gain, A-weighting
THD+N	Total Harmonic Distortion Plus Noise Ratio	-	-60	-	dBA	0dB gain, A-weighting
R_{IN}	Input Resistance	1.5	-	70.5	KΩ	
$Gain_{PGA}$	Programmable Gain Amplifier Range	-9	-	+36	dB	
$Step_{PGA}$	Programmable Gain Amplifier Step	-	1.5	-	dB	
$Gain_{Boost}$	Boost Gain	-	20	-	dB	
Speaker BTL Output @ 8Ω						
SNR	Signal to Noise Ratio	-	80	-	dB	A-weighting

THD+N	Total Harmonic Distortion Plus Noise Ratio	-	-74	-	dB	A-weighting
	Programmable Gain Amplifier Range	-30	-	+6	dB	
	Programmable Gain Amplifier Step Size	-	1.16	-	dB	
	BTL Speaker Output Power	-	380	-	mW	THD @ 10%
		-	200	-	mW	THD @ 1%

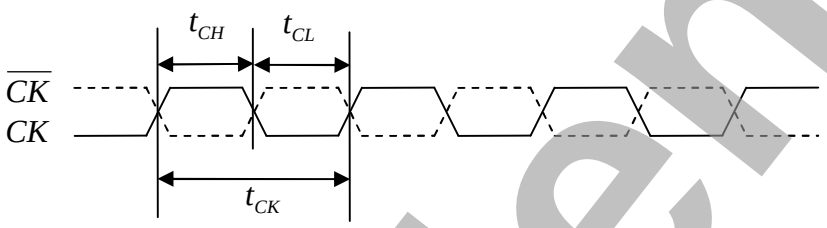
* The SNR of audio output is measured according to AES17-1998 CL 9.3

USB

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
Driver Characteristics						
High speed mode						
t_{HSR}	High speed differential rise time	500	-	-	ps	
t_{HSF}	High speed differential fall time	500	-	-	ps	
Full speed mode						
t_{FR}	Rise time	4	-	20	ns	CL=50pF; 10 to 90% of $\|V_{OH}-V_{OL}\|$
t_{FF}	Fall time	4	-	20	ns	CL=50pF; 90 to 10% of $\|V_{OH}-V_{OL}\|$
t_{FRMA}	Differential rise/fall time matching (t_{FR}/t_{FF})	90	-	110	%	Excluding the first transition from idle mode
V_{CRS}	Output signal crossover voltage	1.3	-	2.0	V	Excluding the first transition from idle mode
Driving timing						
High speed mode						
	Driver waveform requirement	see eye pattern of template 1				Follow template1 described in USB2.0 spec
Full speed mode						
	VI, FSE0, OE to DP, DN propagation delay	-	-	15	ns	for detailed description of VI, FSE0 and OE, please refer to USB1.1 spec
Receiver timing						
High speed mode (template 4, USB2.0 spec)						
	Data source jitter and receiver jitter tolerance	see eye pattern of template 4				Follow template 4 described in USB2.0 spec
Full speed mode						
$t_{PLH(RCV)}$ $t_{PHL(RCV)}$	Receiver propagation delay (DP; DM to RCV)	-	-	15	ns	for detailed description of RCV, please refer to USB1.1 spec
$t_{PLH(single)}$ $t_{PHL(single)}$	Receiver propagation delay (DP; DM to VOP, VON)	-	-	15	ns	

SDRAM

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{CH}	SDRAM clock high pulse width	3	-	-	ns	
t_{CL}	SDRAM clock low pulse width	3	-	-	ns	
t_{SETUP}	SDRAM setup time	3	-	-	ns	
t_{HOLD}	SDRAM hold time	2	-	-	ns	



SDR/DDR SDRAM clock high pulse and low